

2 Mbit / 4 Mbit Firmware Hub

SST49LF002A / SST49LF004A



Advance Information

FEATURES:

- **Firmware Hub for Intel® 810, 810E, 820, 840 Chipsets**
- **2Mbits or 4Mbits SuperFlash memory array for code/data storage**
 - SST49LF002A: 256K x8 (2 Mbit)
 - SST49LF004A: 512K x8 (4 Mbit)
- **Flexible Erase Capability**
 - Uniform 4 KByte Sectors
 - Uniform 32 KByte overlay blocks for SST49LF002A
 - Uniform 64 KByte overlay blocks for SST49LF004A
 - Top boot block protection
 - 32 KByte for SST49LF002A
 - 64 KByte for SST49LF004A
 - Chip-Erase for PP Mode
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption**
 - Active Current: 10 mA (typical)
 - Standby Current: 10 μ A (typical)
- **Fast Sector-Erase/Byte-Program Operation**
 - Sector-Erase Time: 18ms (typical)
 - Block-Erase Time: 18ms (typical)
 - Chip-Erase Time: 70ms (typical)
 - Byte-Program Time: 14 μ s (typical)
 - Chip Rewrite Time:
 - SST49LF002A: 4 seconds (typical)
 - SST49LF004A: 8 seconds (typical)
 - Single-pulse Program or Erase
 - Internal timing generation
- **Two Operational Modes**
 - Firmware Hub Interface (FWH) Mode for in-system operation
 - Parallel Programming (PP) Mode for fast production programming
- **Firmware Hub Hardware Interface Mode**
 - 5-signal communication interface supporting byte Read and Write
 - 33 MHz clock frequency operation
 - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block
 - Block Locking Register for all blocks
 - Standard SDP Command Set
 - Data# Polling and Toggle Bit for End-of-Write detection
 - 5 GPI pins for system design flexibility
 - 4 ID pins for multi-chip selection
- **Parallel Programming (PP) Mode**
 - 11 pin multiplexed address and 8 pin data I/O interface
 - Supports fast In-System or PROM programming for manufacturing
- **CMOS I/O Compatibility**
- **Packages Available**
 - 32-Pin PLCC
 - 32-Pin TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST49LF00xA flash memory devices are designed to be read-compatible to the Intel 82802 Firmware Hub (FWH) device for PC-BIOS application. It provides protection for the storage and update of code and data in addition to adding system design flexibility through five general purpose inputs. Two interface modes are supported by the SST49LF00xA: Firmware Hub (FWH) Interface Mode for In-System programming and Parallel Programming (PP) Mode for fast factory programming of PC-BIOS applications.

The SST49LF00xA flash memory devices are manufactured with SST's proprietary, high performance SuperFlash Technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF00xA devices significantly improve performance and reliability, while lowering power consumption.

The SST49LF00xA devices write (Program or Erase) with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies. The SST49LF00xA products provide a maximum Byte-Program time of 20 μ sec. The entire memory can be erased and programmed byte-by-byte typically in 8 seconds, when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore



the system software or hardware does not have to be calibrated or correlated to the cumulated number of Erase cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles.

To protect against inadvertent write, the SST49LF00xA devices have on-chip hardware and software data (SDP) protection schemes. It is offered with typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

To meet high density, surface mount requirements, the SST49LF00xA device is offered in 32-pin TSOP and 32-pin PLCC packages. See Figures 1 and 2 for pinouts and Table 5 for pin descriptions.

Mode Selection and Description

The SST49LF00xA flash memory devices can operate in two distinct interface modes: the Firmware Hub Interface (FWH) mode and the Parallel Programming (PP) mode. The IC (Interface Configuration pin) is used to set the interface mode selection. If the IC pin is set to logic High, the device is in PP mode; while if the IC pin is set Low, the device is in the FWH mode. The IC selection pin must be configured prior to device operation. In FWH mode, the device is configured to interface with its host using Intel's Firmware Hub proprietary protocol. Communication between Host and the SST49LF00xA occurs via the 4-bit I/O communication signals, FWH [3:0] and the FWH4. In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The column addresses are mapped to the higher internal addresses, and the row addresses are mapped to the lower internal addresses. See Device Memory Map for address assignments.

FIRMWARE HUB (FWH) MODE

Device Operation

The FWH mode uses a 5-signal communication interface, FWH[3:0] and FWH4, to control operations of the SST49LF00xA. Operations such as Memory Read and Memory Write uses Intel FWH propriety protocol. JEDEC Standard SDP (Software Data Protection) Byte-Program, Sector-Erase and Block-Erase command sequences are incorporated into the FWH memory cycles. Chip-Erase is only available in PP Mode.

The device enters standby mode when FWH4 is high and no internal operation is in progress. The device is in ready mode when FWH4 is low and no activity is on the FWH bus.

Abort Mechanism

If FWH4 is driven low for one or more clock cycles during a FWH cycle, the cycle will be terminated and the device will wait for the ABORT command. The host must drive the FWH[3:0] with '1111b' (ABORT command) to return the device to ready mode. If abort occurs during the internal write cycle, the data may be incorrectly programmed or erased. It is required to wait for the Write operation to complete prior to initiation of the abort command. It is recommended to check the write status with Data# Polling (DQ₇) or Toggle Bit (DQ₆) pins. One other option is to wait for the fixed write time to expire.

Device Memory Hardware Write Protection

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF00xA. The TBL# pin is used to write protect 16 boot sectors (64 KBytes) at the highest flash memory address range for the SST49LF004A and 8 boot sectors (32 KBytes) for SST49LF002A. WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot sectors. When TBL# pin is held high, write protection of the top boot sectors is then determined by the Boot Block Locking register. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results.

TBL# is internally ORed with the top Boot Block Locking register. When TBL# is low, the top Boot Block is hardware write protected regardless of the state of the Write-Lock bit for the Boot Block Locking register. Clearing the write protect bit in the register when TBL# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

WP# is internally ORed with the Block Locking register. When WP# is low, the blocks are hardware write protected regardless of the state of the Write-Lock bit for the corresponding Block Locking registers. Clearing the write protect bit in any register when WP# is low will have no functional effect, even though the register may indicate that the block is no longer locked.



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TABLE 1: GENERAL PURPOSE INPUTS REGISTER

Bit	Function	32-PLCC Pin#	32-TSOP Pin#
7:5	Reserved	-	-
4	FGPI[4] Reads status of general purpose input pin	30	7
3	FGPI[3] Reads status of general purpose input pin	3	15
2	FGPI[2] Reads status of general purpose input pin	4	16
1	FGPI[1] Reads status of general purpose input pin	5	17
0	FGPI[0] Reads status of general purpose input pin	6	18

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Reset

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization.

During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, FWH[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time T_{RSTP} . A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 14, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered had been disrupted from an incomplete Erase or Program operation.

Multiple Device Selection

The four ID pins, ID[3:0], allow multiple devices to be attached to the same bus by using different ID strapping in a system. When the SST49LF00xA is used as a boot device, ID[3:0] must be strapped as 0000, all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). The SST49LF00xA will compare the strapping values, if there is a mismatch, the device will ignore the remainder of the cycle and go into standby mode. For further information regarding FWH device mapping and paging, please refer to the Intel 82801 (ICH) I/O Controller Hub documentation. Since there is no ID support in PP Mode, to program multiple devices a stand-alone PROM programmer is recommended.

REGISTERS

There are three types of registers available on the SST49LF00xA, the General Purpose Inputs Register, Block Locking Registers and the JEDEC ID Registers. These registers appear at their respective address loca-

tion in the 4 GBytes system memory map. Unused register locations will read as 0x00. Any attempt to read or write any registers during internal write operation will be ignored.

General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of FGPI[4:0] pins at power-up on the SST49LF00xA. It is recommended that the FGPI[4:0] pins are in the desired state before FWH4 is brought low for the beginning of the bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI register for the boot device appears at FFBC0100H in the 4 GBytes system memory map, and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in Erase/Program operation. Refer to the relevant application note for details. See Table 1 for the GPI_REG bits and function.

Block Locking Registers

The SST49LF00xA offers software control lock protection through the Block Locking registers. The Block Locking registers are read/write registers and it is accessible through standard addressable memory locations listed in Table 2. There are 8 blocks for both the SST49LF002A and SST49LF004A devices. Each block has its own Block Locking register.

Write Lock

The Write-Lock bit, bit 0, controls the lock state described in Table 3. The default write status of all blocks after power-up is write locked. When bit 0 of the Block Locking register is set, Program and Erase operations for the corresponding block are prevented. Clearing the Write-Lock bit will unprotect the block. The Write-Lock bit must be cleared prior to starting a Program or Erase operation since it is sampled at the beginning of the operation.



TABLE 2: BLOCK LOCKING REGISTERS

Register	Memory Address	
	SST49LF002A	SST49LF004A
Block 7 (Boot Block)	FFBF8002H	FFBF0002H
Block 6 Register	FFBF0002H	FFBE0002H
Block 5 Register	FFBE8002H	FFBD0002H
Block 4 Register	FFBE0002H	FFBC0002H
Block 3 Register	FFBD8002H	FFBB0002H
Block 2 Register	FFBD0002H	FFBA0002H
Block 1 Register	FFBC8002H	FFB90002H
Block 0 Register	FFBC0002H	FFB80002H

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TABLE 3: BLOCK LOCKING REGISTER BITS

Reserved Bit [7..2]	Lock-Down Bit [1]	Write-Lock Bit [0]	Lock Status
000000	0	0	Full Access
000000	0	1	Write Locked (Default State at Power-Up)
000000	1	0	Locked Open (Full Access Locked Down)
000000	1	1	Write Locked Down

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The Write-Lock bit functions in conjunction with the hardware Write Lock pin TBL# for the top Boot Block. When TBL# is low, it overrides the software locking scheme. The top Boot Block Locking register does not indicate the state of the TBL# pin.

The Write-Lock bit functions in conjunction with the hardware WP# pin for blocks 0 to 6. When WP# is low, it overrides the software locking scheme. The Block Locking register does not indicate the state of the WP# pin.

Lock Down

The Lock-Down bit, bit 1, controls the Block Locking register as described in Table 3. When in the FWH interface mode, the default Lock Down status of all blocks upon power-up is not locked down. Once the Lock-Down bit is set, any future attempted changes to that Block Locking register will be ignored. The Lock-Down bit is only cleared upon a device reset with RST# or INIT# or power down. Current Lock Down status of a particular block can be determined by reading the corresponding Lock-Down bit. Once a block's Lock-Down bit is set, the Write-Lock bits for that block can no longer be modified, and the block is locked down in its current state of write accessibility.

JEDEC ID Registers

The JEDEC ID registers for the boot device appear at FFBC0000H and FFBC0001H in the 4 GBytes system memory map, and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in Erase/Program operation. Unused register location will read as 0x00. Refer to the relevant application note for details. See Table 4 for device ID code.

PARALLEL PROGRAMMING MODE

Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Read

The Read operation of the SST49LF00xA device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 7, for further details.

Reset

A V_{IL} on RST# pin initiates a device reset.



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Byte-Program Operation

The SST49LF00xA device is programmed on a byte-by-byte basis. The Byte-Program operation is initiated by executing a four-byte-command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte-Program operation, the row address (A10-A0) is latched on the falling edge of R/C# and the column Address (A21-A11) is latched on the rising edge of R/C#. The data bus is latched in the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 μ s. See Figure 8 for Program operation timing diagram, Figure 11 for timing waveforms, and Figure 19 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 12 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size for the SST49LF004A and 32 KByte uniform block size for the SST49LF002A. The Block-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Block-Erase command (50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 13 for timing waveforms. Any commands written during the Block-Erase operation will be ignored.

Chip-Erase

The SST49LF00xA device provides a Chip-Erase operation only in PP Mode, which allows the user to erase the entire memory array to the "1's" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 7 for the command sequence, Figure 14 for timing diagram, and Figure 22 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST49LF00xA device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ₇)

When the SST49LF00xA device is in the internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 9 for Data# Polling timing diagram and Figure 20 for a flowchart.

Toggle Bit (DQ₆)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next



operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figure 10 for Toggle Bit timing diagram and Figure 20 for a flowchart.

Data Protection

The SST49LF00xA device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST49LF00xA provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., program and erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST49LF00xA device is shipped with the Software Data Protection permanently enabled. See Table 7 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Electrical Specifications

The AC and DC specifications for the FWH Interface signals (FWH[3:0], CLK, FWH4, and RST#) as defined in Section 4.2.2 of the "PCI Local Bus Specification, Rev. 2.1". Refer to Table 8 for the DC voltage and current specifications. Refer to Tables 13, 14, 16 and 17 for the AC timing specifications for Clock, Read, Program, Erase and Reset operations.

Product Identification Mode

The product identification mode identifies the device as the SST49LF00xA and manufacturer as SST.

TABLE 4: PRODUCT IDENTIFICATION TABLE

	Byte	Data	JEDEC ID Address Location
Manufacturer's ID	0000 H	BF H	FFBC0000H
Device ID			
SST49LF002A	0001 H	57H	FFBC0001H
SST49LF004A	0001 H	60H	FFBC0001H

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Design Considerations

SST recommends a high frequency 0.1 μF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 μF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 μF next to each socket.

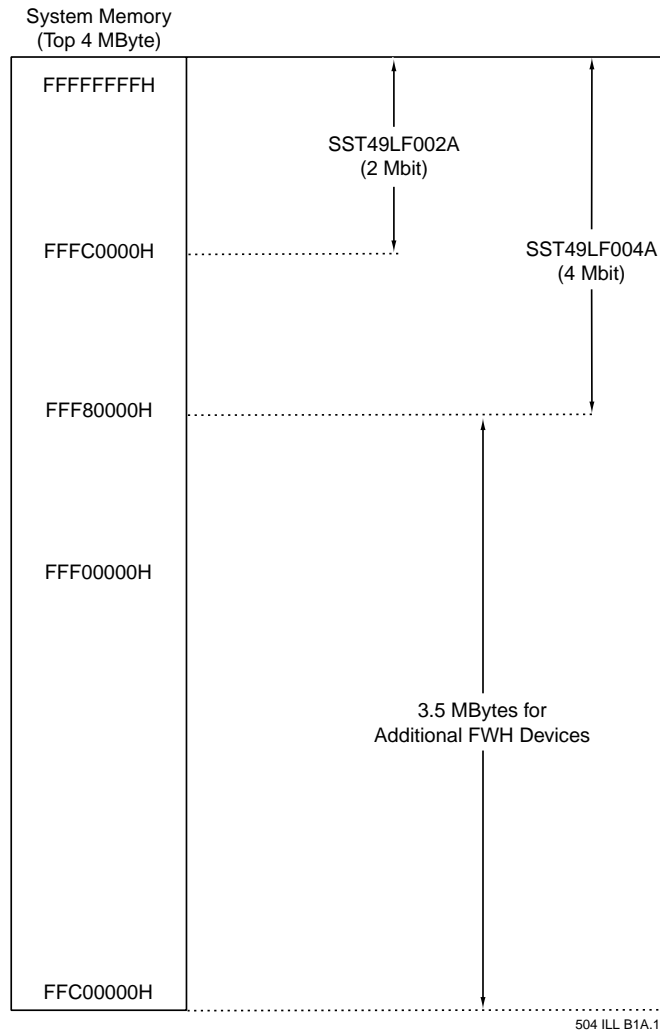
The RST# pin must remain stable at V_{IH} for the entire duration of an Erase operation. WP# must remain stable at V_{IH} for the entire duration of the Erase and Program operations for non-boot block sectors. To write data to the top boot block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the Erase and Program operations.



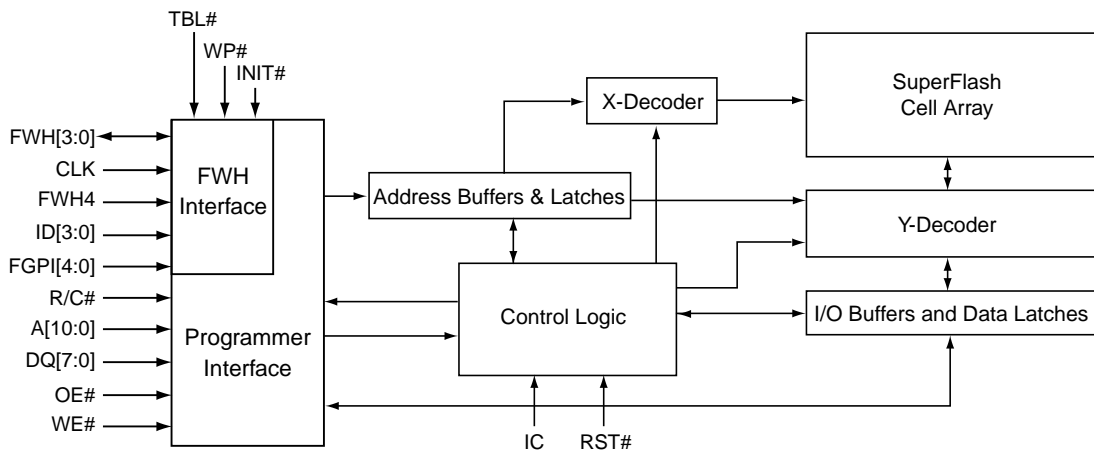
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BOOT-CONFIGURATION SYSTEM MEMORY MAP

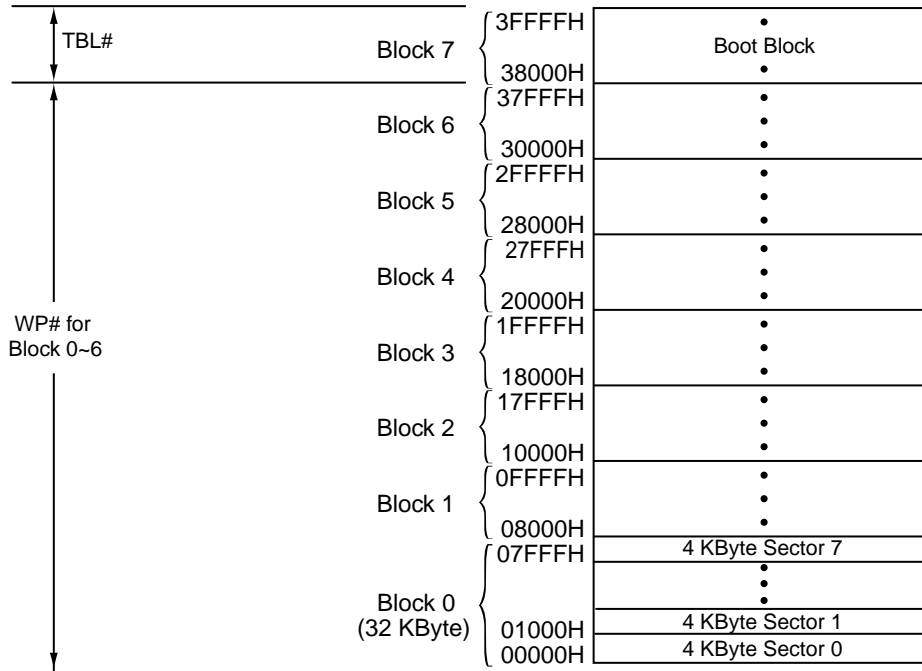


FUNCTIONAL BLOCK DIAGRAM



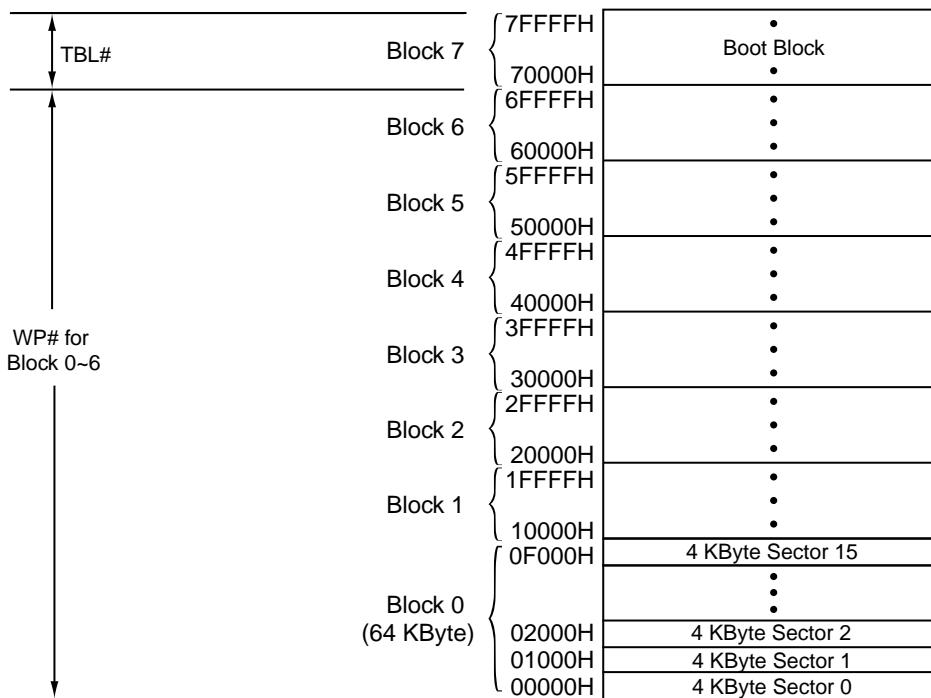


DEVICE MEMORY MAP FOR SST49LF002A



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DEVICE MEMORY MAP FOR SST49LF004A



504 ILL F45.4



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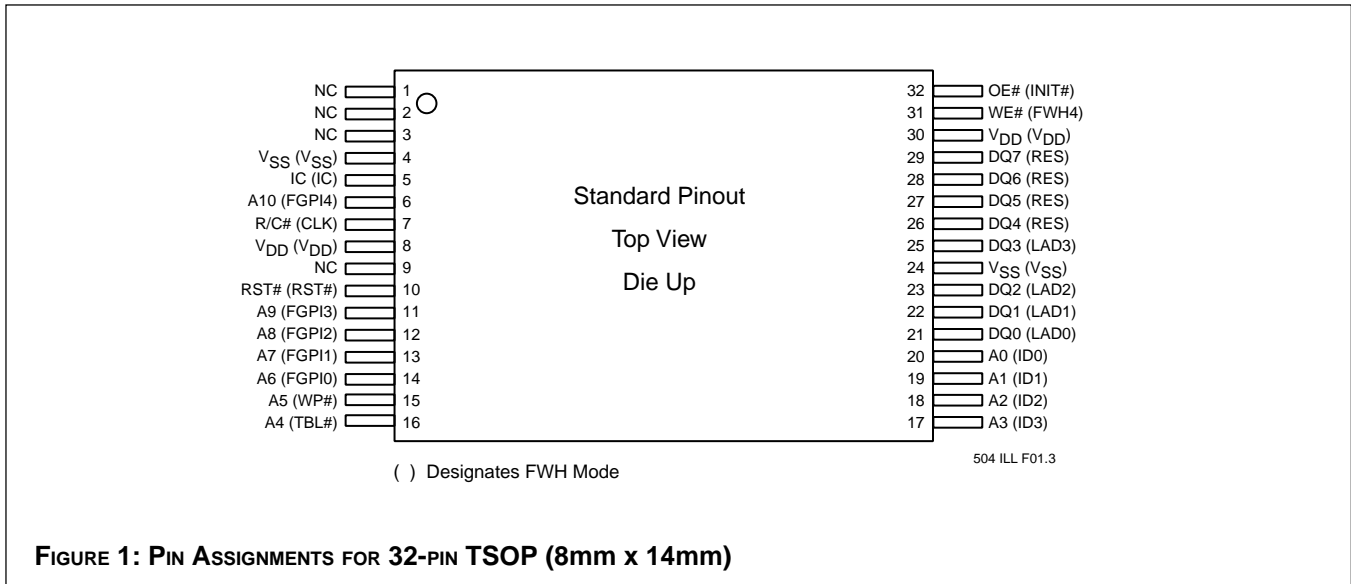


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP (8mm x 14mm)

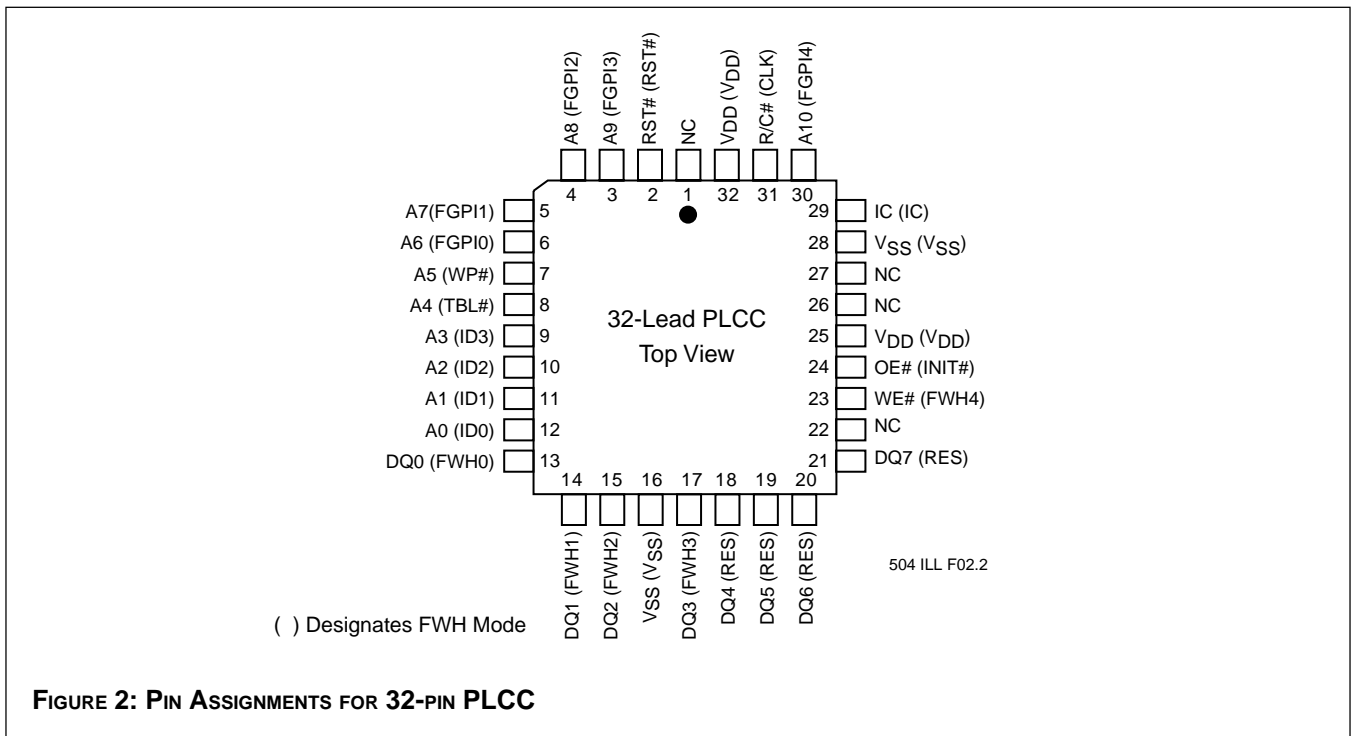


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLCC



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TABLE 5: PIN DESCRIPTION

Symbol	Pin Name	Type ¹	Interface		Functions
			PP	FWH	
A ₁₀ -A ₀	Address	I	X		Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
DQ ₇ -DQ ₀	Data	I/O	X		To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
OE#	Output Enable	I	X		To gate the data output buffers.
WE#	Write Enable	I	X		To control the Write operations.
IC	Interface Configuration Pin	I	X	X	This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, FWH mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin is internally pulled-down with a resistor between 20-100 KΩ
INIT#	Initialize	I		X	This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited.
ID[3:0]	Identification Inputs	I		X	These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0] = 0000 and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ
FGPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through GPI_REG register. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	I		X	When low, prevents programming to the boot block sectors at top of memory. When TBL# is high it disables hardware write protection for the top block sectors.
FWH[3:0]	FWH I/Os	I/O		X	I/O Communications
CLK	Clock	I		X	To provide a clock input to the control unit
FWH4	FWH Input	I		X	Input Communications
RST#	Reset	I	X	X	To reset the operation of the device
WP#	Write Protect	I		X	When low, prevents programming to all but the highest addressable blocks. When WP# is high it disables hardware write protection for these blocks.
R/C#	Row/Column Select	I	X		Select For the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses.
RES	Reserved			X	Not implemented. Reserved for future use.
V _{DD}	Power Supply	I	X	X	To provide power supply (3.0-3.6V)
V _{SS}	Ground	I	X	X	Circuit ground (OV reference)
NC	No Connection	I	X	X	Unconnected pins.

Note 1. I = Input, O = Output

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TABLE 6: OPERATION MODES SELECTION (PP Mode)

Mode	RST#	OE#	WE#	DQ	Address
Read	V _{IH}	V _{IL}	V _{IH}	D _{OUT}	A _{IN}
Program	V _{IH}	V _{IH}	V _{IL}	D _{IN}	A _{IN}
Erase	V _{IH}	V _{IH}	V _{IL}	X	Sector or Block address, XXh for Chip-Erase
Reset	V _{IL}	X	X	High Z	X
Write Inhibit	V _{IH}	V _{IL}	X	High Z/D _{OUT}	X
	X	V _{IH}		High Z/D _{OUT}	X
Product Identification	V _{IH}	V _{IL}	V _{IH}	Manufacturer ID (BF) Device ID ⁽⁷⁾	A ₁₈ - A ₁ = V _{IL} , A ₀ = V _{IL} A ₁₈ - A ₁ = V _{IL} , A ₀ = V _{IH}

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TABLE 7: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st ⁽⁶⁾ Write Cycle		2nd ⁽⁶⁾ Write Cycle		3rd ⁽⁶⁾ Write Cycle		4th ⁽⁶⁾ Write Cycle		5th ⁽⁶⁾ Write Cycle		6th ⁽⁶⁾ Write Cycle	
	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA ⁽³⁾	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA _x ⁽²⁾	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA _x ⁽⁵⁾	50H
Chip-Erase ⁽⁹⁾	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry ^(7,8)	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

Notes:

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- (1) Address format A₁₄-A₀ (Hex), Addresses A₁₅-A₂₁ are a "Don't Care" for the Command sequence.
- (2) SA_x for Sector-Erase Address
- (3) BA = Program Byte address
- (4) Both Software ID Exit operations are equivalent
- (5) BA_x for Block-Erase Address
- (6) FWH Mode use consecutive Write cycles to complete a command sequence;
PP Mode use consecutive bus cycles to complete a command sequence.
- (7) SST Manufacturer ID = BFH, is read with A₀ = 0,
With A₁₇-A₁ = 0; 49LF002A Device ID = 57H, is read with A₀ = 1.
With A₁₈-A₁ = 0; 49LF004A Device ID = 60H, is read with A₀ = 1.
- (8) The device does not remain in Software Product ID Mode if powered down.
- (9) Chip-Erase is supported in PP Mode only



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Advance Information

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{DD} + 0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to $V_{DD} + 1.0V$
Package Power Dissipation Capability ($T_A = 25^\circ C$)	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ⁽¹⁾	50 mA

Note: ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	3 ns
Output Load	$C_L = 30$ pF
See Figures 17 and 18	

TABLE 8: DC OPERATING CHARACTERISTICS (ALL INTERFACE)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current Read		12	mA	OE# = V_{IL} , WE# = V_{IH} , All I/Os open, Address input = V_{IL}/V_{IH} , at $F = 1/T_{RC}$ Min., $V_{DD} = V_{DD}$ Max
	Write		15	mA	
I_{SB}	Standby V_{DD} Current (FWH Interface)		100	μA	FWH4 = 0.9 V_{DD} , f = 33 MHz $V_{DD} = V_{DD}$ Max, All other inputs $\geq 0.9 V_{DD}$ or $\leq 0.1 V_{DD}$
I_{RY} ⁽¹⁾	Ready Mode V_{DD} Current (FWH Interface)		10	mA	FWH4 = V_{IL} , f = 33 MHz $V_{DD} = V_{DD}$ Max All other inputs $\geq 0.9 V_{DD}$ or $\leq 0.1 V_{DD}$
I_i	Input Current for IC, ID [3:0] pins		200	μA	$V_{IN} = GND$ to V_{DD} , $V_{DD} = V_{DD}$ Max
I_{LI}	Input Leakage Current		1	μA	$V_{IN} = GND$ to V_{DD} , $V_{DD} = V_{DD}$ Max
I_{LO}	Output Leakage Current		1	μA	$V_{OUT} = GND$ to V_{DD} , $V_{DD} = V_{DD}$ Max
V_{IHI}	INIT# Input High Voltage	1.0	$V_{DD} + 0.5$	V	$V_{DD} = V_{DD}$ Max
V_{ILI}	INIT# Input Low Voltage	-0.5	0.4	V	$V_{DD} = V_{DD}$ Max
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	$V_{DD} = V_{DD}$ Min
V_{IH}	Input High Voltage	0.5 V_{DD}	$V_{DD} + 0.5$	V	$V_{DD} = V_{DD}$ Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	$I_{OL} = 1500\mu A$, $V_{DD} = V_{DD}$ Min
V_{OH}	Output High Voltage	0.9 V_{DD}		V	$I_{OH} = -500\mu A$, $V_{DD} = V_{DD}$ Min

Note: (1) The device is in Ready Mode when no activity is on the FWH bus.

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TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^{(1)}$	Power-up to Read Operation	100	μs
$T_{PU-WRITE}^{(1)}$	Power-up to Write Operation	100	μs

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 10: PIN IMPEDANCE ($V_{DD} = 3.3V$, $T_a = 25^\circ C$, $f=1$ Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^{(2)}$	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
$C_{IN}^{(2)}$	Input Capacitance	$V_{IN} = 0V$	12 pF
$L_{PIN}^{(3)}$	Pin Inductance		20 nH

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Note: (2) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

(3) Refer to PCI spec.

TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^{(4)}$	Endurance	10,000	Cycles	JEDEC Standard A117
$T_{DR}^{(4)}$	Data Retention	100	Years	JEDEC Standard A103
$V_{ZAP_HBM}^{(4)}$	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
$V_{ZAP_MM}^{(4)}$	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
$I_{LTH}^{(4)}$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

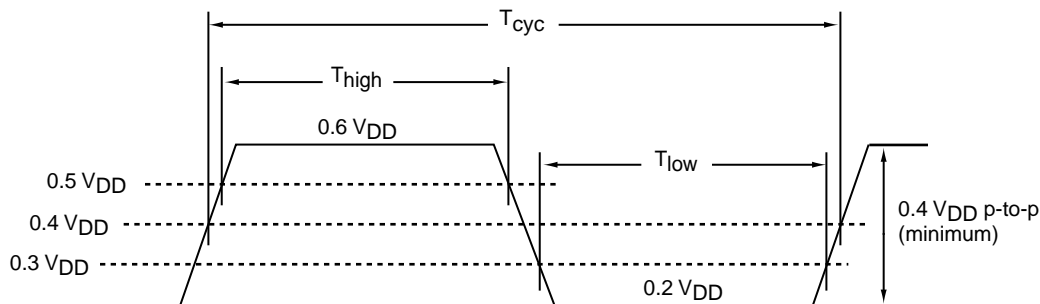
504 PGM T11.2

Note: (4) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: CLOCK TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{CYC}	CLK Cycle Time	30		ns
T_{HIGH}	CLK High Time	11		ns
T_{LOW}	CLK Low Time	11		ns
–	CLK Slew Rate (peak-to-peak)	1	4	V/ns
–	RST# or INIT# Slew Rate	50		mV/ns

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504 ILL F27.0

FIGURE 3: CLK WAVEFORM



AC CHARACTERISTICS (FWH MODE)

TABLE 13: READ/WRITE CYCLE TIMING PARAMETERS (FWH MODE), $V_{DD} = 3.0-3.6V$

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
$T_{VAL}^{(1)}$	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		20	μs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms
T_{ON}	Clock Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)		28	ns

Note: (1) Minimum and maximum times have different loads. See PCI spec.

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TABLE 13A: AC INPUT/OUTPUT SPECIFICATIONS (FWH MODE)

Symbol	Parameter	Min	Max	Units	Conditions
$I_{OH}(AC)$	Switching Current High	$-12V_{DD}$	Equation C ⁽³⁾	mA	$0 < V_{OUT} \leq 0.3V_{DD}$
		$-17.1(V_{DD}-V_{OUT})$			$0.3V_{DD} < V_{OUT} < 0.9V_{DD}$
					$0.7V_{DD} < V_{OUT} < V_{DD}$
	(Test Point)		$-32V_{DD}$	mA	$V_{OUT} = 0.7V_{DD}$
$I_{OL}(AC)$	Switching Current Low	$16V_{DD}$	Equation D ⁽³⁾	mA	$V_{DD} > V_{OUT} \geq 0.6V_{DD}$
		$-17.1(V_{DD}-V_{OUT})$			$0.6V_{DD} > V_{OUT} > 0.1V_{DD}$
					$0.18V_{DD} > V_{OUT} > 0$
	(Test Point)		$38V_{DD}$	mA	$V_{OUT} = 0.18V_{DD}$
I_{CL}	Low Clamp Current	$-25+(V_{IN}+1)/0.015$		mA	$-3 < V_{IN} \leq -1$
I_{CH}	High Clamp Current	$25+(V_{IN}-V_{DD}-1)/0.015$		mA	$V_{DD}+4 > V_{IN} \geq V_{DD}+1$
$slew_r^{(2)}$	Output Rise Slew Rate	1	4	V/ns	$0.2V_{DD}-0.6V_{DD}$ load
$slew_f^{(2)}$	Output Fall Slew Rate	1	4	V/ns	$0.6V_{DD}-0.2V_{DD}$ load

Note: (2) PCI specification output load is used.

(3) See PCI spec.

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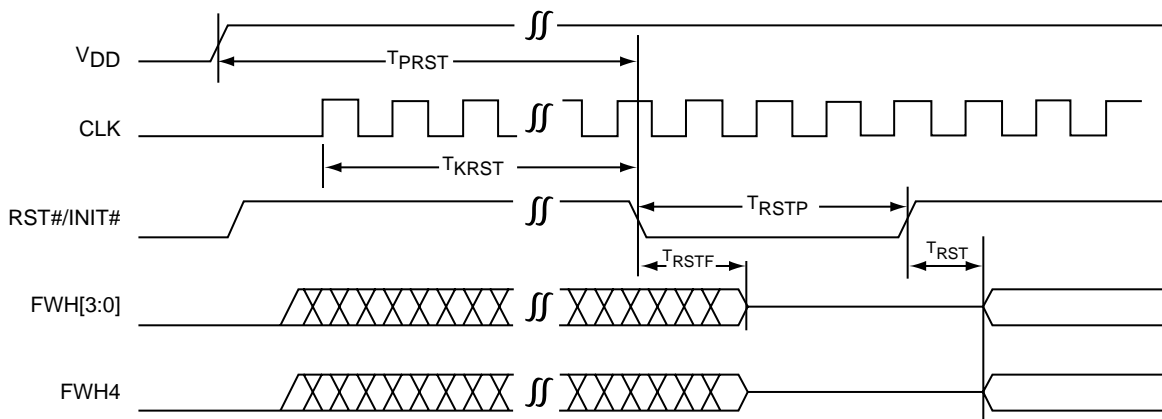
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Advance Information

TABLE 14: RESET TIMING PARAMETERS, $V_{DD} = 3.0-3.6V$

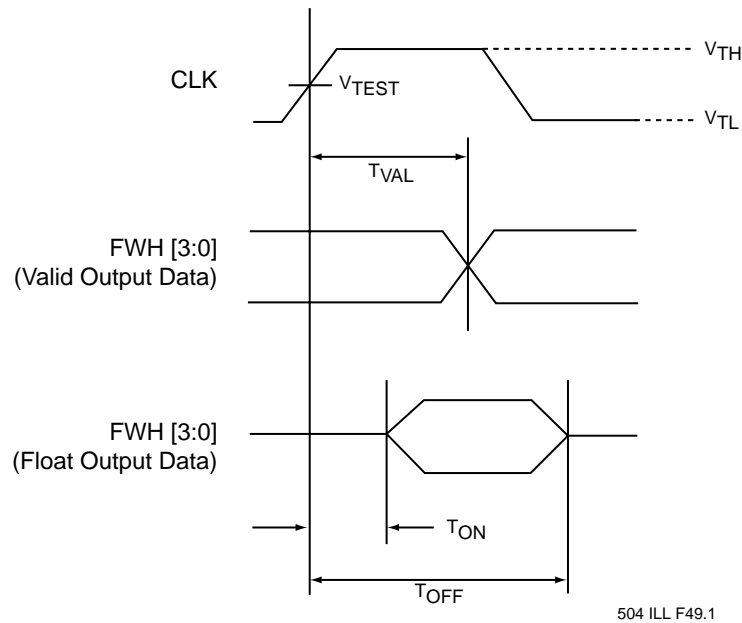
Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Active	1		ms
T_{KRST}	Clock Stable to Reset Active	100		μs
T_{RSTP}	Reset Pulse Width	100		ns
T_{RSTF}	Reset Active to Output Float		50	ns
T_{RST}	Reset Inactive to Input Active		10	μs

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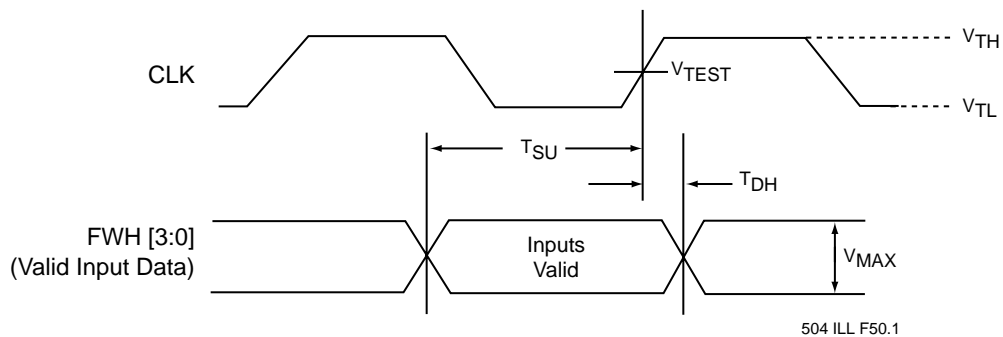
504 ILL F51.0

FIGURE 4: RESET TIMING DIAGRAM



504 ILL F49.1

FIGURE 5: OUTPUT TIMING PARAMETERS



504 ILL F50.1

FIGURE 6: INPUT TIMING PARAMETERS

TABLE 15: INTERFACE MEASUREMENT CONDITION PARAMETERS

Symbol	Value	Units
$V_{TH}^{(1)}$	0.6 V_{DD}	V
$V_{TL}^{(1)}$	0.2 V_{DD}	
$V_{TEST}^{(1)}$	0.4 V_{DD}	
V_{MAX}	0.4 V_{DD}	
Input Signal Edge Rate	1 V/ns	

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Note: (1) The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL} . Timing parameters must be met with no more overdrive than this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.



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Advance Information

AC CHARACTERISTICS (PP MODE)

TABLE 16: READ CYCLE TIMING PARAMETERS $V_{DD} = 3.0-3.6V$ (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		ms
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

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TABLE 17: PROGRAM/ERASE CYCLE TIMING PARAMETERS $V_{DD} = 3.0-3.6V$ (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		ms
T_{AS}	R/C# Address Setup Time	50		ns
T_{AH}	R/C# Address Hold Time	50		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		40	ns
T_{OET}	OE# to Toggle Bit Delay		40	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		20	μ s
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms

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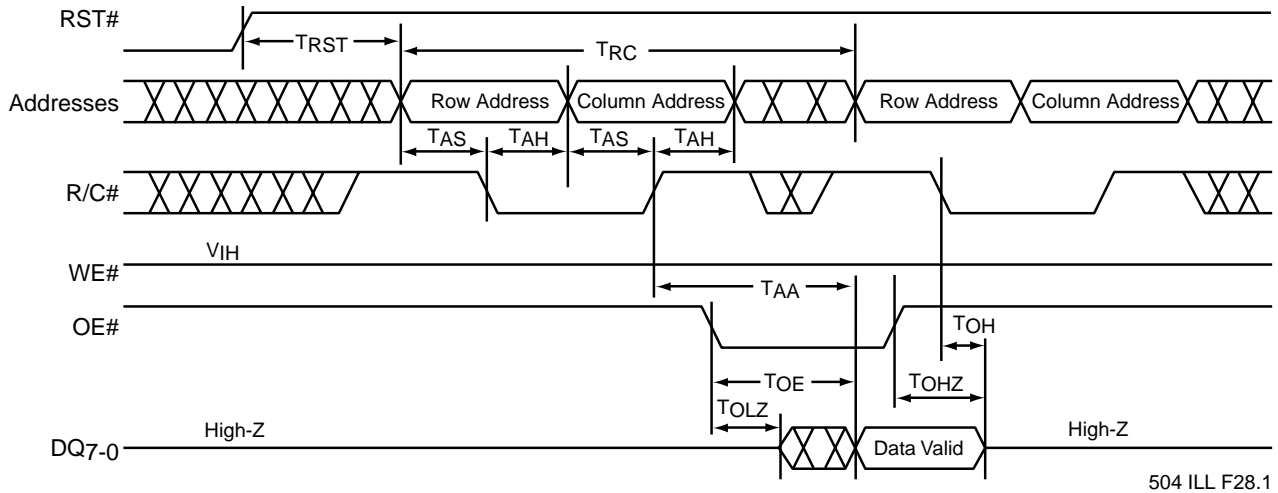


FIGURE 7: READ CYCLE TIMING DIAGRAM (PP MODE)

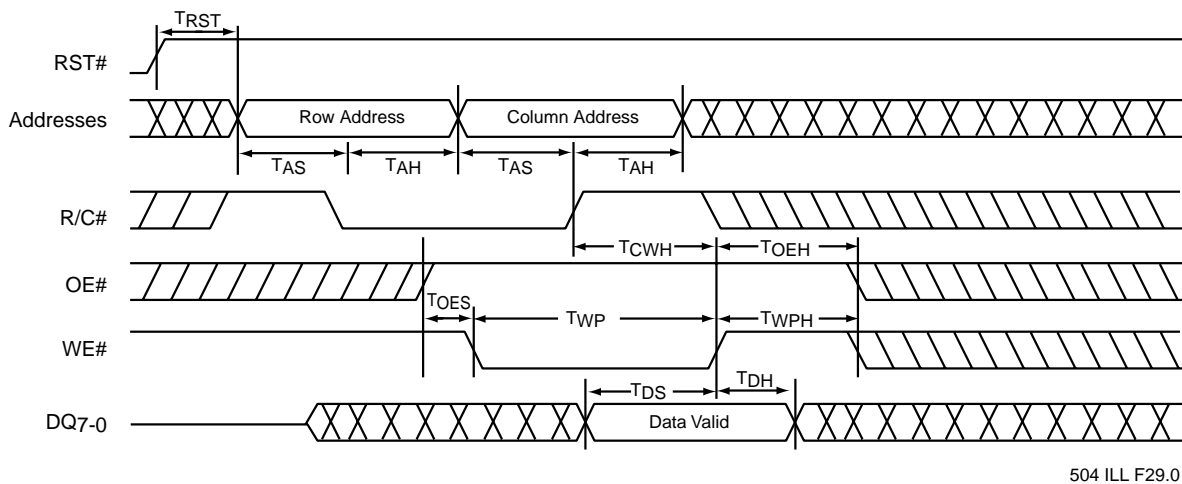


FIGURE 8: WRITE CYCLE TIMING DIAGRAM (PP MODE)



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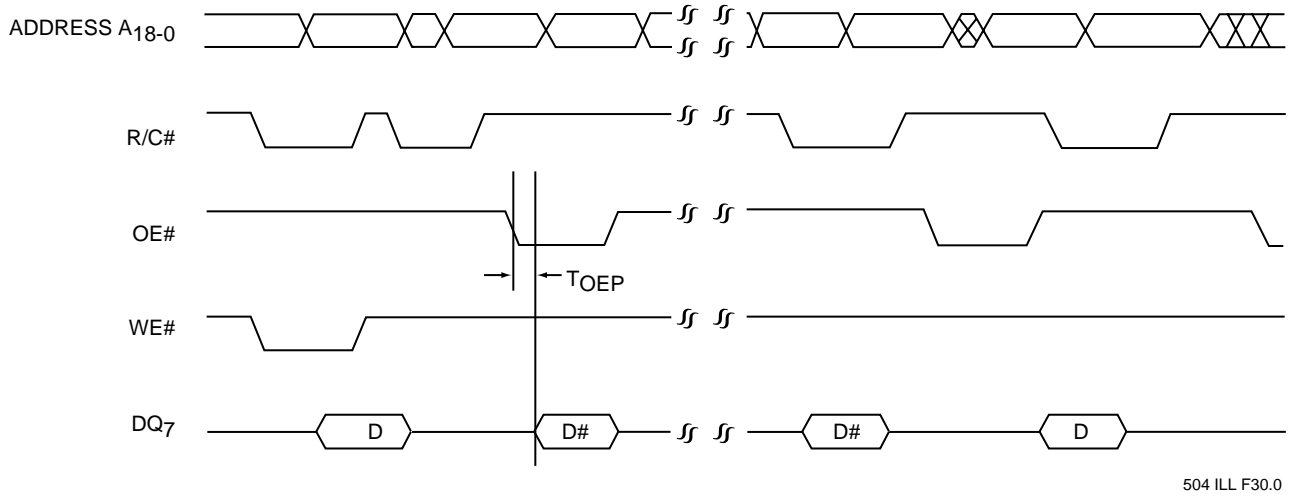


FIGURE 9: DATA# POLLING TIMING DIAGRAM (PP MODE)

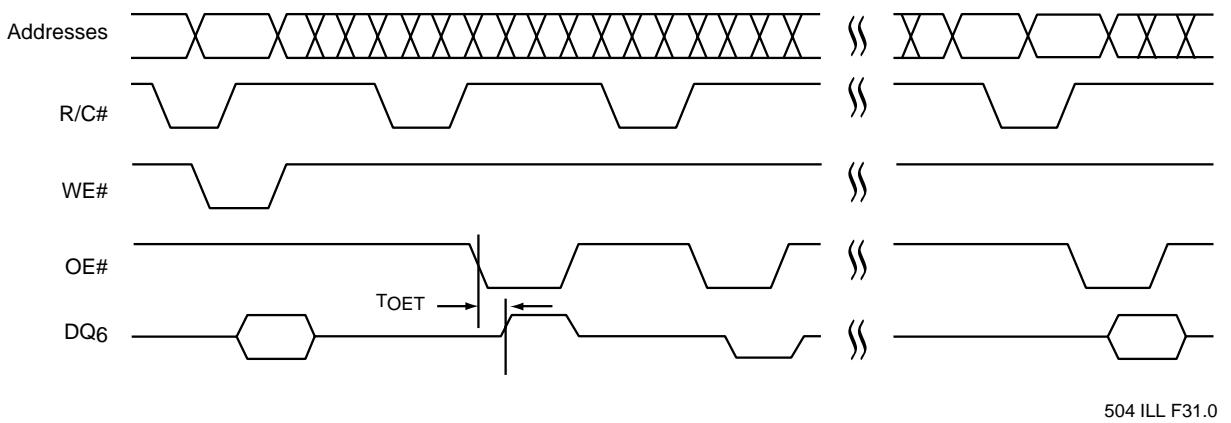


FIGURE 10: TOGGLE BIT TIMING DIAGRAM (PP MODE)

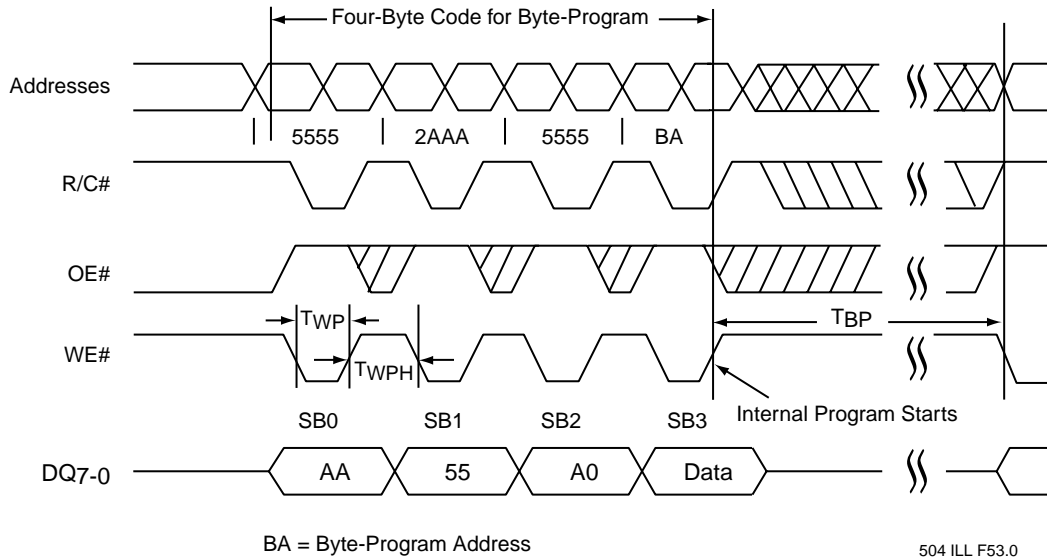


FIGURE 11: BYTE-PROGRAM TIMING DIAGRAM (PP MODE)

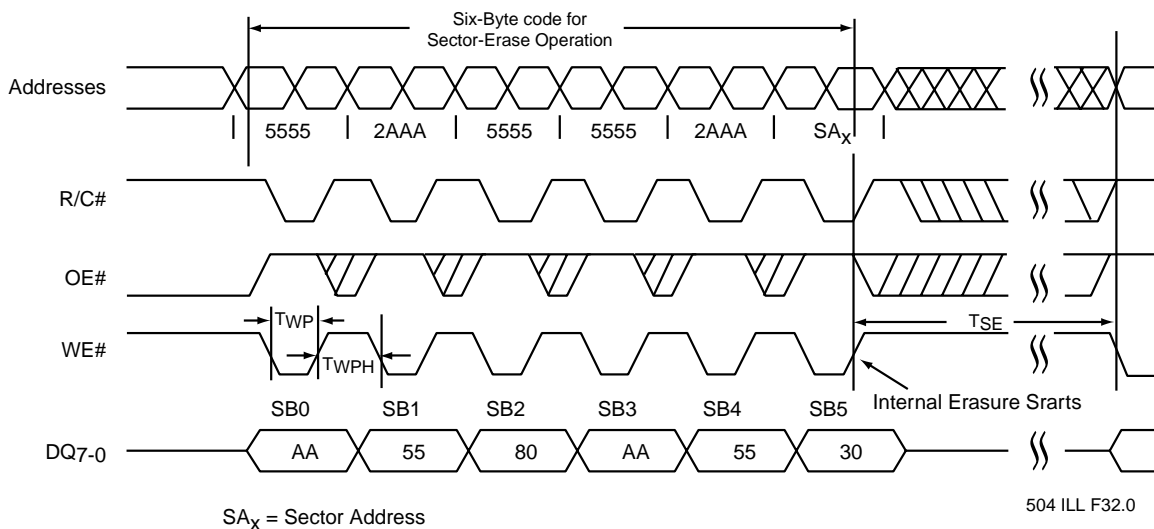


FIGURE 12: SECTOR-ERASE TIMING DIAGRAM (PP MODE)



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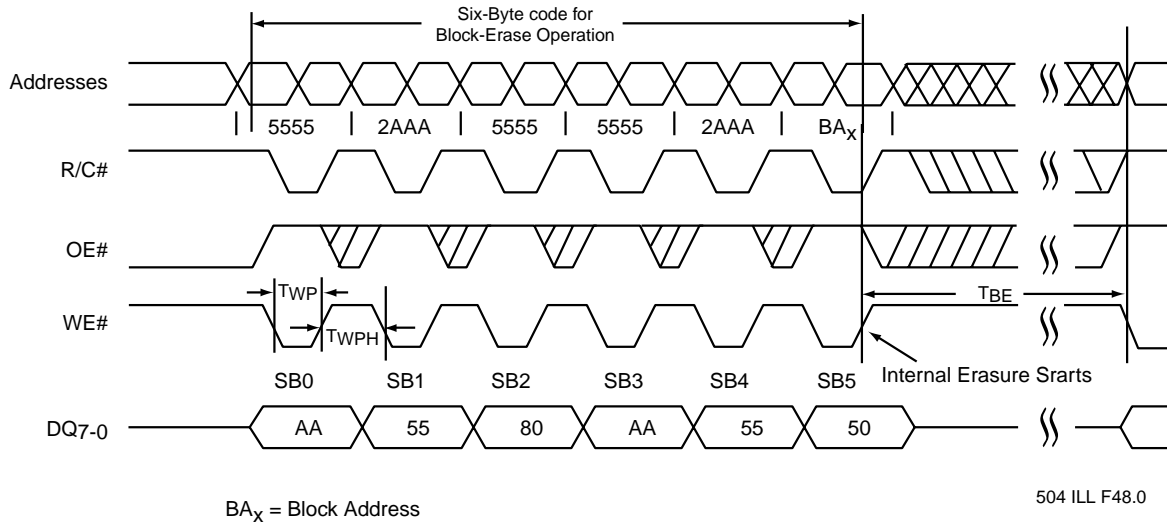


FIGURE 13: BLOCK-ERASE TIMING DIAGRAM (PP MODE)

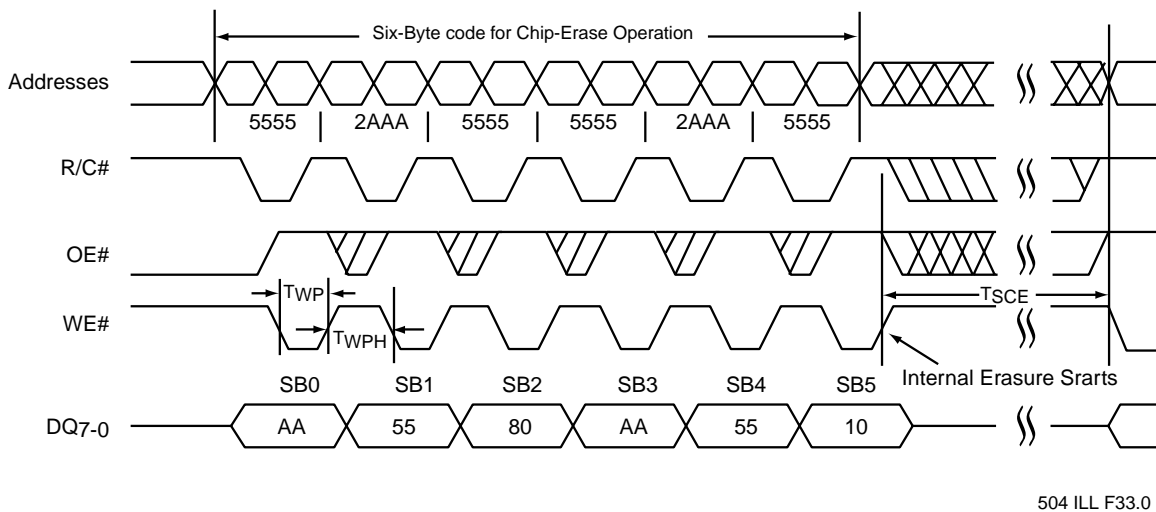


FIGURE 14: CHIP-ERASE TIMING DIAGRAM (PP MODE)

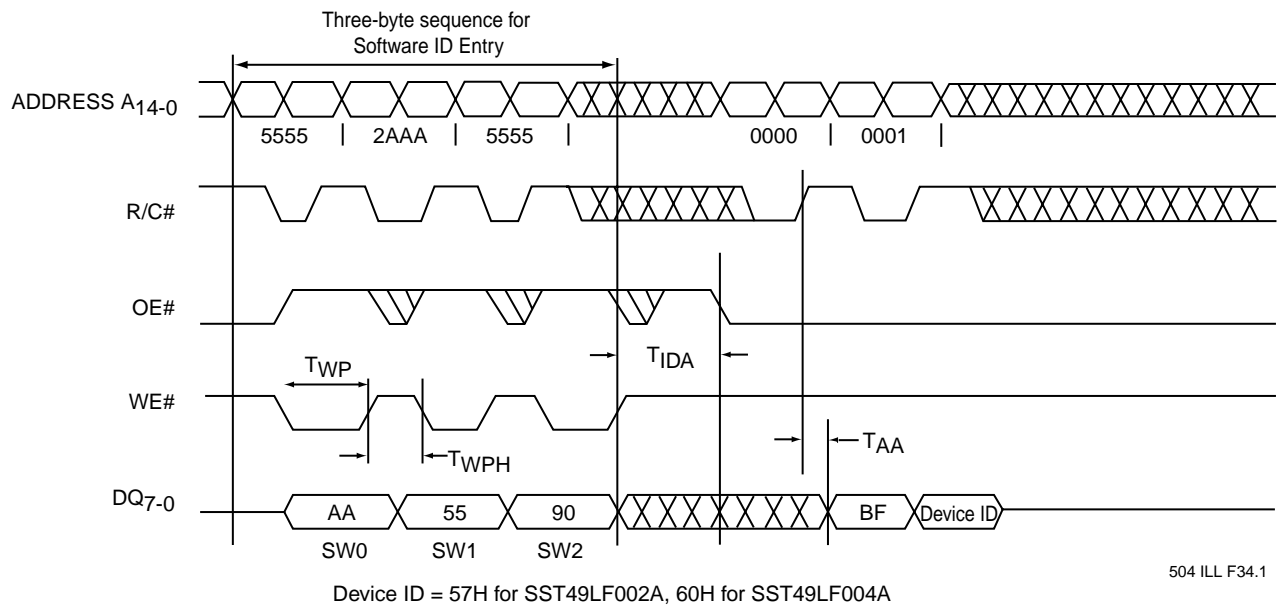


FIGURE 15: SOFTWARE ID ENTRY AND READ (PP MODE)

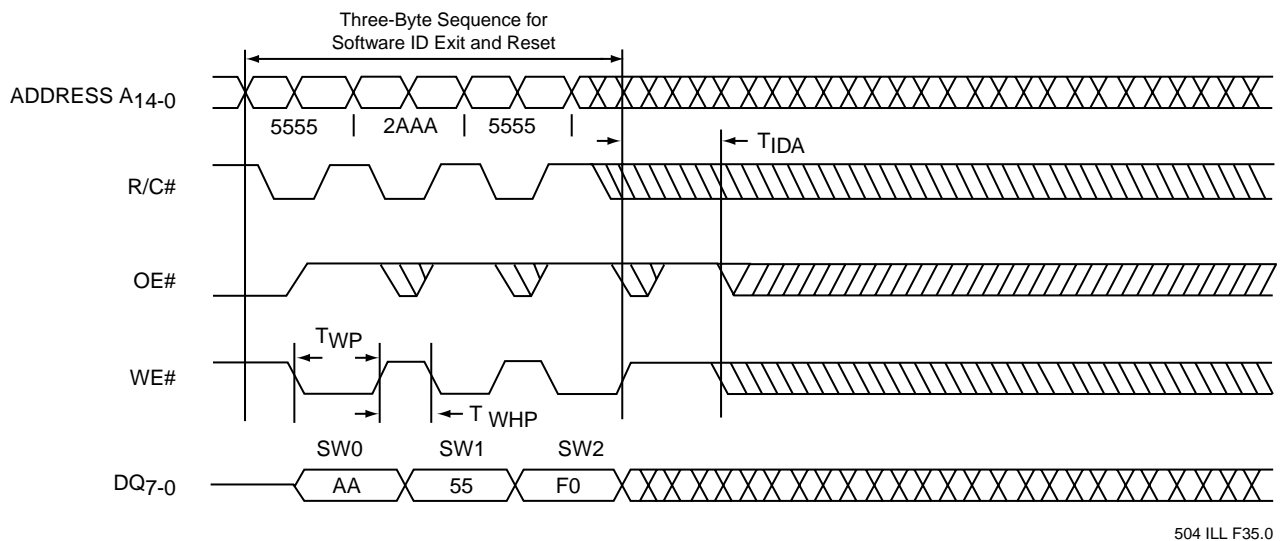


FIGURE 16: SOFTWARE ID EXIT AND RESET (PP MODE)



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Advance Information

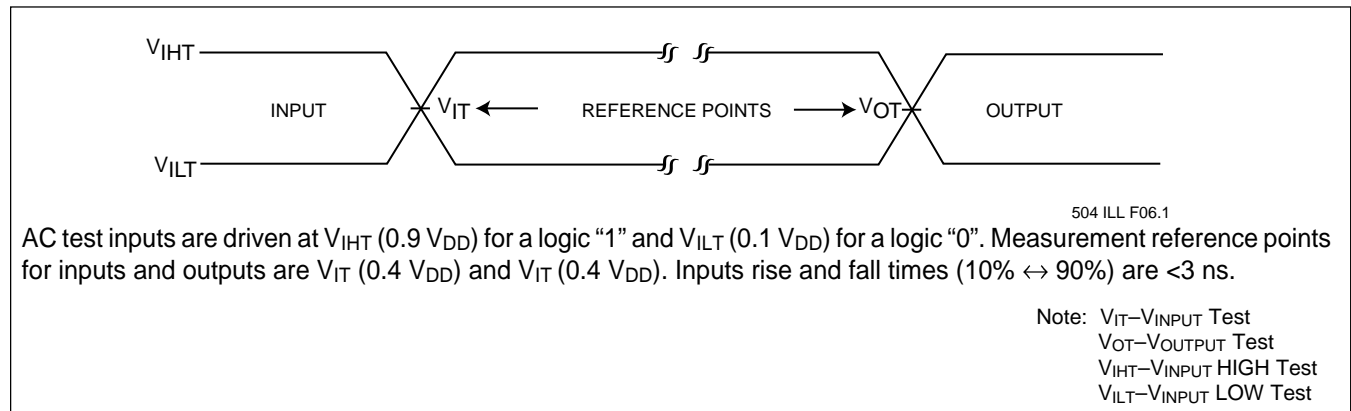


FIGURE 17: AC INPUT/OUTPUT REFERENCE WAVEFORMS (PP MODE)

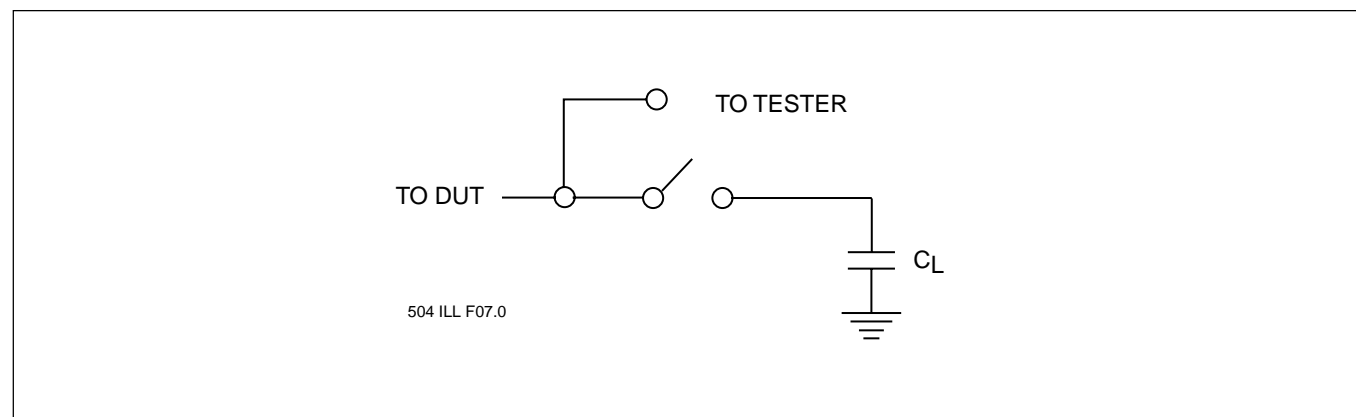


FIGURE 18: A TEST LOAD EXAMPLE (PP MODE)

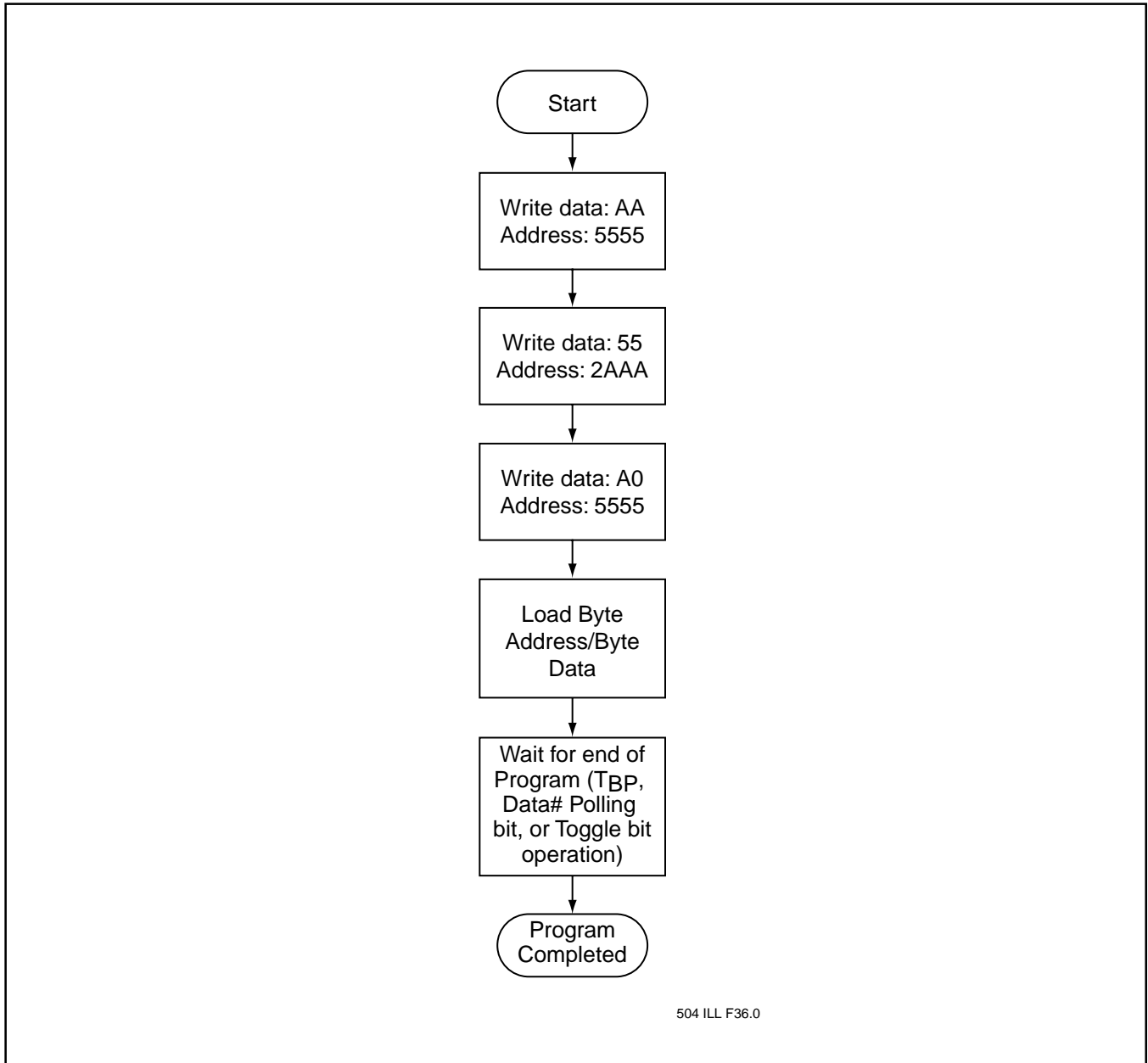


FIGURE 19: BYTE-PROGRAM ALGORITHM



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Advance Information

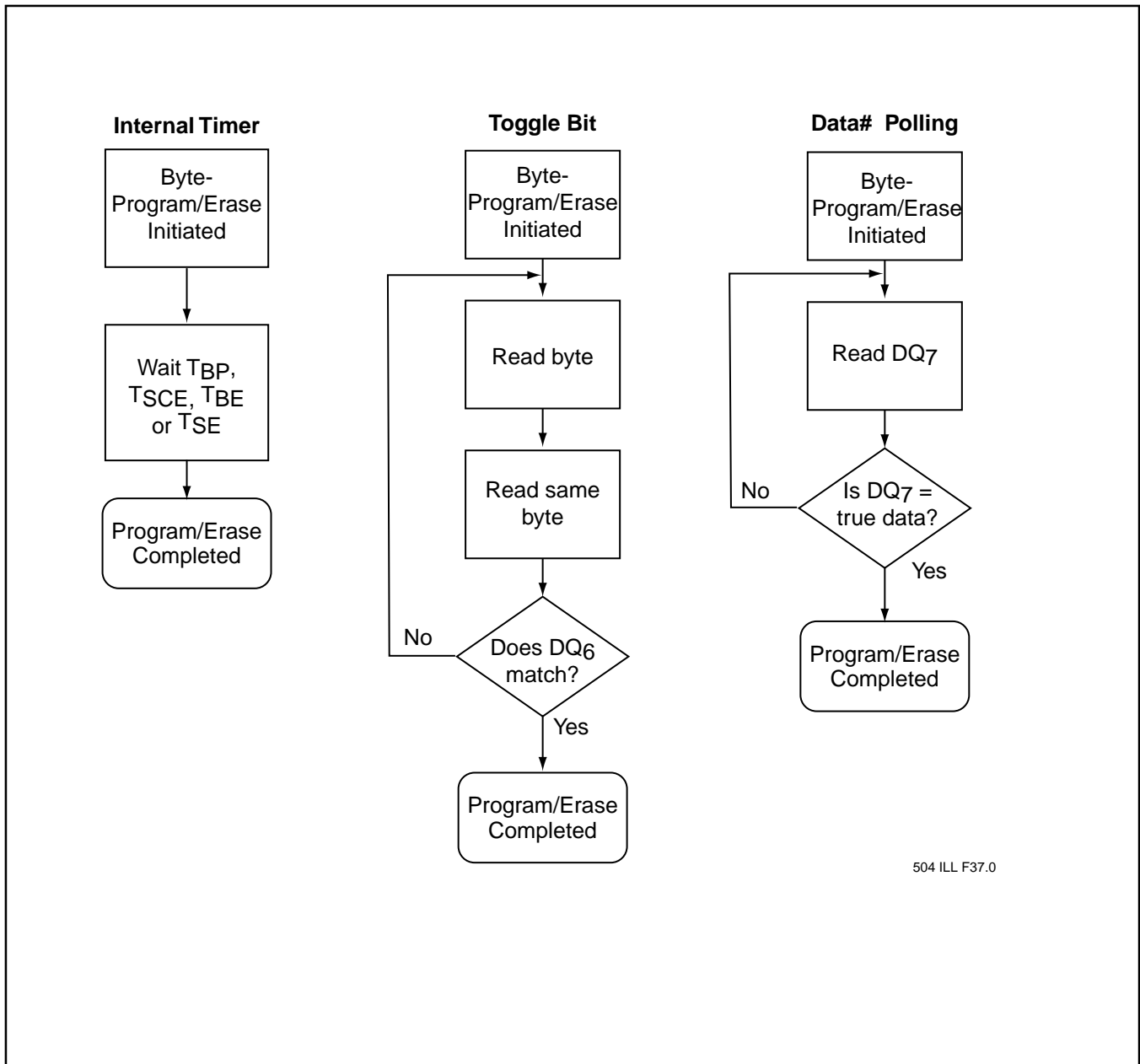
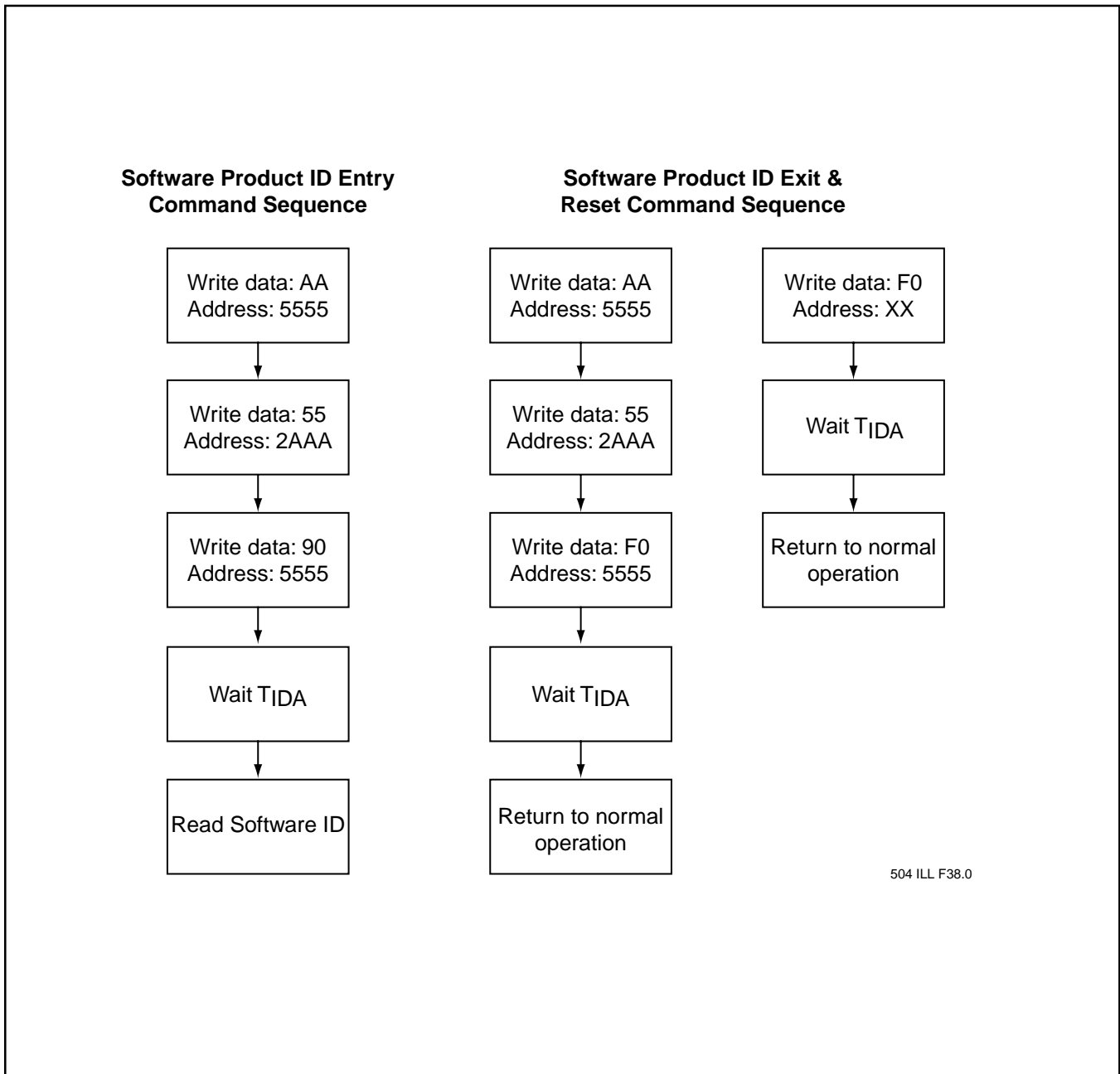


FIGURE 20: WAIT OPTIONS



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FIGURE 21: SOFTWARE PRODUCT COMMAND FLOWCHARTS



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Advance Information

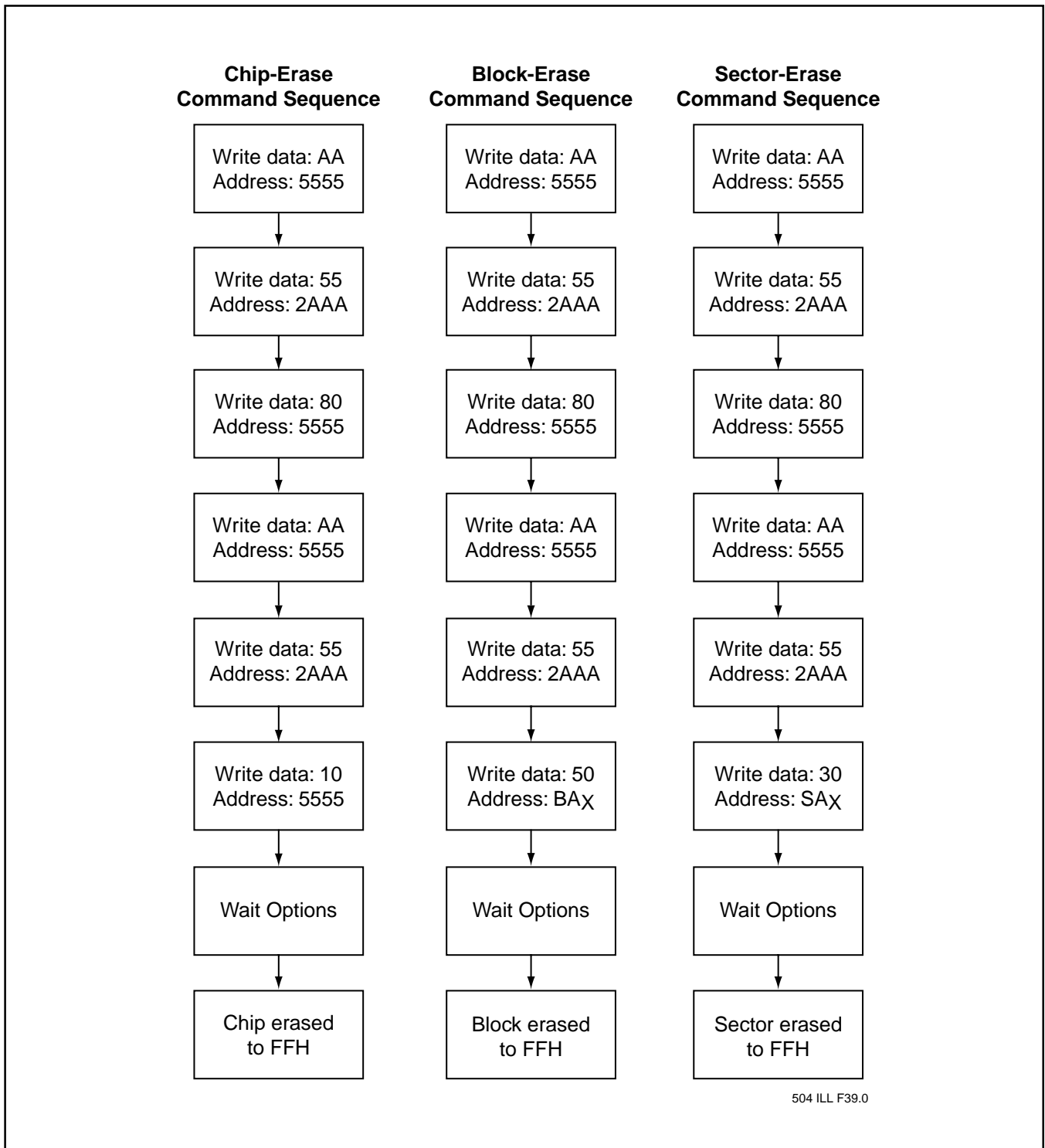


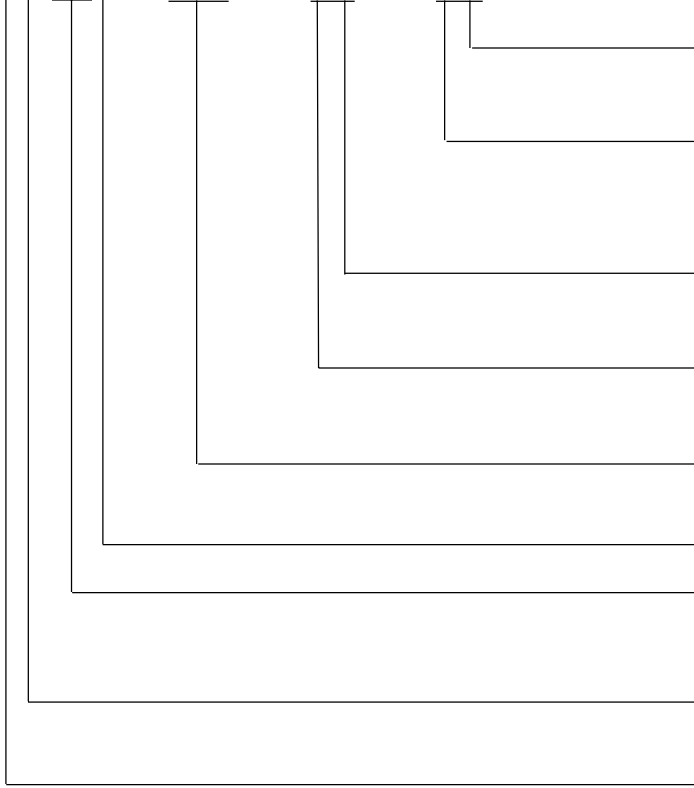
FIGURE 22: ERASE COMMAND SEQUENCE



PRODUCT ORDERING INFORMATION

Device Speed Suffix1 Suffix2

SST49LF00xA - XXX - XX - XX



Package Modifier

H = 32 pins

Package Type

N = PLCC

W = TSOP (die up) (8mm x 14mm)

Operating Temperature

C = Commercial = 0° to 85°C

Minimum Endurance

4 = 10,000 cycles

Serial Access Clock Frequency

33 = 33 MHz

Version

Density

002 = 2 Mbits

004 = 4 Mbits

Voltage Range

L = 3.0-3.6V

Device Family

SST49LF002A Valid combinations

SST49LF002A-33-4C-WH

SST49LF002A-33-4C-NH

SST49LF004A Valid combinations

SST49LF004A-33-4C-WH

SST49LF004A-33-4C-NH

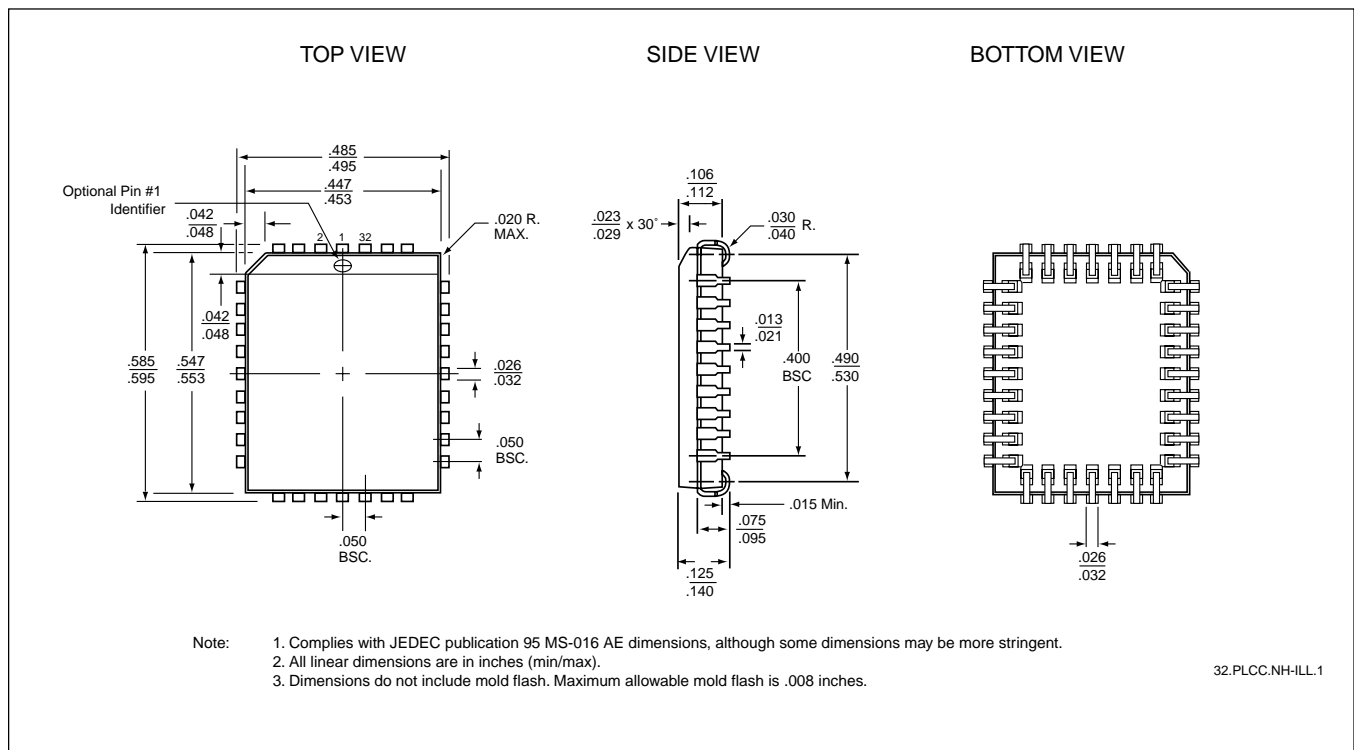
Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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Advance Information

PACKAGING DIAGRAMS



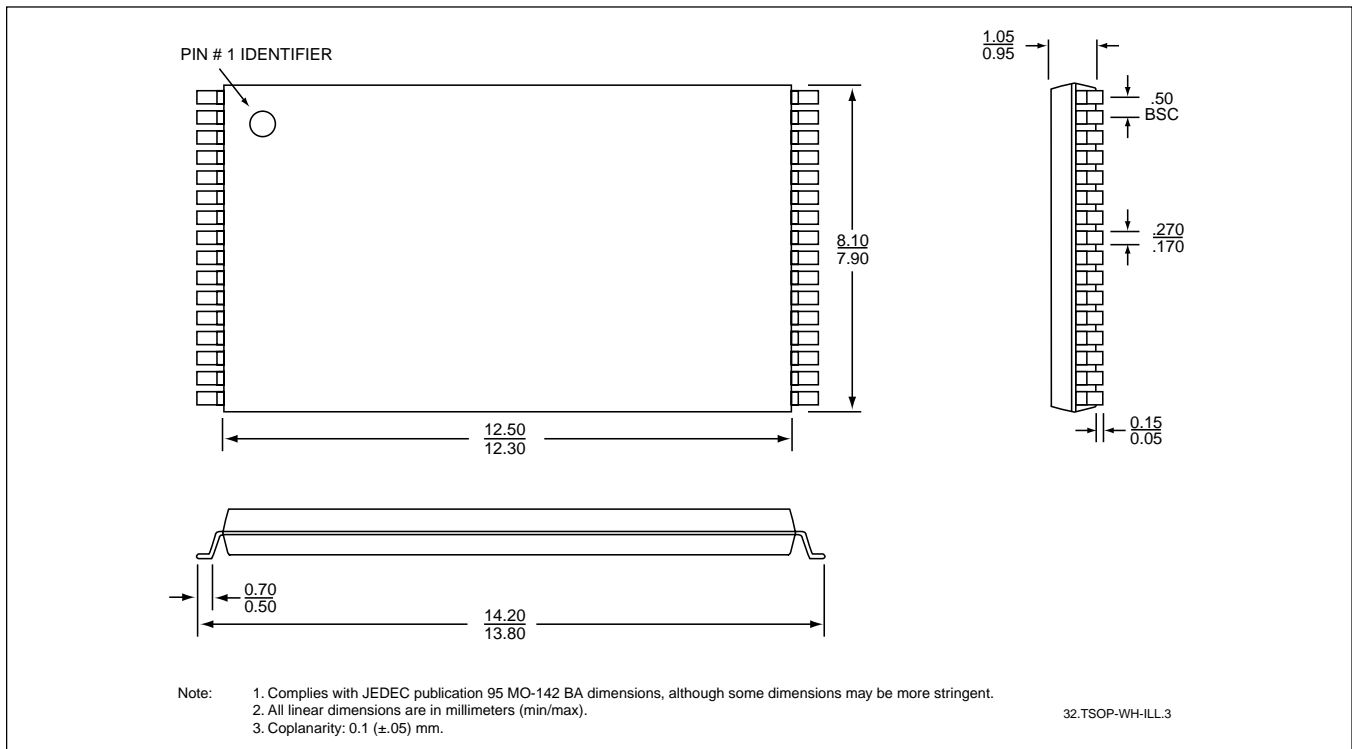
32-PIN PLASTIC LEAD CHIP CARRIER (PLCC)

SST PACKAGE CODE: NH



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Advance Information



32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH